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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Ryo Kubota

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02/03/2005

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
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EXAMINER

LEE, HSIEN MING

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/817,233

Applicant(s)

KUBOTA ET AL.

Examiner

Hsien-ming Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7,9 and 12-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7,9 and 12-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Remarks

1. The objection to claim 22 is withdrawn.
2. Claims 1-7, 9 and 12-23 are pending in the application.

Claim Objections

3. Claim 23 is objected to because of the following informalities: at line 6, "said drove" should be – said groove -- . Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Sung (US 5,858,831).

In re claim 23, Sung teaches providing a CMOS logic circuit portion 50 and a DRAM portion 60 on a substrate 1;

- forming a transistor 7/9c/16/17/18/20b/26/27/28 on a substrate 1 (Fig. 10);
- forming an interlayer film 29 and 34 on the substrate 1 to cover the first transistor 7/9c/16/17/18/20b/26/27/28 (Fig. 18);
- forming a groove 36 in the interlayer film 29/34 (Fig.18);

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- forming a first polysilicon film 37 on an upper surface of the interlayer film 34/29 and a second polysilicon film 37 on an inner wall of the groove 36 (Fig. 18);
- forming a first HSG on a surface of the first polysilicon film 37 at the CMOS logic portion 50 and a second HSG on a surface of the second polysilicon film 37 at the DRAM portion 60 (col. 7, lines 52-54);
- removing the first HSG and the first polysilicon film 37 from the CMOS logic circuit portion 50 by a CMP process to expose the upper surface of the interlayer film 34 while leaving the second HSG in the groove 36 (col. 8, lines 4-8 and Fig.18);
- forming a capacitor dielectric film 38 on the second HSG film in the groove 36 and on the exposed surface of the interlayer film 29/34 (col. 7, lines 52-54 and Fig. 18); and
- forming an upper electrode 39 on the capacitor dielectric film 38 (Fig.18).

Grounds of Rejections

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-7, 9 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (US 5,858,831) in view of applicants' admitted prior art ("AAPA") and JP H11-284139 (submitted by the applicant).

In re claims 1-3, 5-7 and 16-18, Sung teaches the claimed method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit 50 and a DRAM 60 on a same semiconductor chip (col. 1, lines 64-67), comprising:

- providing a CMOS logic circuit portion 50 and a DRAM portion 60 of a substrate 1;
- forming a first transistor 7/9c/16/17/18/20b/26/27/28 on the substrate 1 at the CMOS logic circuit portion 50 (Fig. 10);
- forming a second transistor 7/9b/16/17/18/20b on a substrate 1 at the DRAM portion 60 (Fig. 10);
- forming an interlayer film 29 and 34 on the substrate 1 at the CMOS logic circuit portion 50 and on the substrate 1 at the DRAM portions 60, covering the first transistor and the second transistor (Fig. 18);
- forming a groove 36 in the interlayer film 29/34 by removing a portion of the interlayer film 29/34 at the DRAM portion 60 (Fig. 18);
- forming a first polysilicon film 37 on an upper surface of the interlayer film 34/29 at the CMOS logic circuit portion 50 and at the DRAM portions 60, and a second polysilicon film 37 on an inner wall of the groove 36 at the DRAM portion 60 (Fig. 18);
- forming a first HSG on a surface of the first polysilicon film 37 at the CMOS logic portion 50 and a second HSG on a surface of the second polysilicon film 37 at the DRAM portion 60 (col. 7, lines 52-54);
- removing the first HSG and the first polysilicon film 37 *from the CMOS logic circuit portion 50* by a CMP process to expose the top surface of the interlayer film 34 and

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- retaining at least a portion of the HSG in the groove 36 and at least a portion of the polysilicon 37 in the groove 36 (col. 8, lines 4-8 and Fig.18);
- forming a capacitor dielectric film 38 on the second HSG film in the groove 36 and on the exposed surface of the interlayer film 29/34 (col. 7, lines 52-54 and Fig. 18); and
 - forming an upper electrode 39 on the capacitor dielectric film 38 (Fig.18).

Sung also teaches that forming the first and the second transistors include forming a first 7 (thickness: 40~60 Å) and a second gate insulating layer 8 (thickness: 50~70 Å) (Fig. 8; col. 4, lines 21-25); the second transistor comprises a peripheral circuit transistor and a switching transistor, wherein both transistor have similar structure; wherein the step of forming the interlayer film 34/29 comprises the steps of forming a first silicon oxide 29 and a second silicon oxide 34 film; the method further comprising the steps of forming an opening in the first interlayer 29 over a diffusion region 31 of the switching transistor (Fig. 15); forming a capacitor electrode 33 in the opening in the first interlayer film 29 (Fig.17), wherein the capacitor electrode 33 is connected to the diffusion region 31 of the switching transistor (Fig. 17); the groove 36 is formed in the second interlayer film 34 (Fig. 17) and the second polysilicon 37 is connected to the capacitor electrode 33 (Fig. 18); forming a capacitor film 38 on the first HSG film (not shown); and forming an upper electrode 39 on the capacitor film 38 (Fig. 19);

Sung also inherently teaches a step of “ removing said first HSG and said first polysilicon film” as recited in claim 1. The first HSG and the first polysilicon film 37 is formed on the surface of the interlayer film 34 outside the groove 36 (It is a *processing consequence* of the polysilicon layer 37 deposition and HSG formation, col. 7, lines 47-54.); and the second

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polysilicon film 37 is formed on the inner wall of the groove 36 at the DRAM portion 60. As illustrated in Fig. 18, said first HSG and said first polysilicon film have been removed from the surface of the interlayer 34 and only the second polysilicon film 37 and the second HSG are left in the groove 36.

Sung does *not* teach forming a capacitor dielectric film 38 on the second HSG film *after removing* the first HSG and the first polysilicon film *from the CMOS logic portion*.

However, JP H11-284139, in an analogous art as admitted in the specification page 7, first paragraph, teach forming a groove 40 in interlayer film 44 (Fig.4); forming a first polysilicon film 50 on upper surface of the interlayer film 44; forming a first HSG 52 on a surface of the first polysilicon film 50 and a second HSG 52 on a surface of the second polysilicon film within the groove 40 (Fig.4); forming a sacrificial film 54 over the first HSG 52 on the upper surface of the interlayer film 44 and over the second HSG 52 within the groove 40 (Fig.5); removing the first HSG 52 and the first polysilicon 50 from the upper surface of the interlayer film 44A (Fig.6); removing the remaining sacrificial film 54; and **then** forming a capacitor dielectric film 56 **after removing** the first HSG 52 and the first polysilicon film 50 from the upper surface of the interlayer film 44A (Fig.7); and forming an upper electrode 58 on the capacitor dielectric film 56 (Fig.7).

JP H11-284139 further teaches that the interlayer film 44 is formed **at the CMOS side** because the invention is applied to a device comprising both a P-MOS and a N-MOS (second paragraph, page 9, English version). In other words, when removing the first HSG 52 and the first polysilicon film 50 from the upper surface of the interlayer film 44, it also means removing the first HSG 52 and the first polysilicon film 50 from the CMOS portion. Accordingly, the step

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of forming the capacitor dielectric film 56 is performed **after removing** the first HSG 52 and the first polysilicon film 50 **from the CMOS portion**.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to modify Sung's method by **first** removing the first HSG and the first polysilicon from the CMOS portion **prior to** forming the capacitor dielectric film, as taught by JP-H11-284139, and **then** proceed the step of forming the capacitor dielectric film, since by this manner it would form a satisfactory crown-type capacitor.

In re claim 22, Sung also teaches that the step of *removing first HSG and the first polysilicon 37 comprises a step of exposing a part of the interlayer film 29/34* (i.e. exposing the upper surface of the interlayer film 29/34) via a CMP process (col. 8, lines 4-8). Sung in view of JP-H11-284139 also teach that the step of forming said capacitor dielectric film comprises a step of forming a first capacitor dielectric film 38 on said part of said interlayer film 34/29 and a second capacitor dielectric film 38 on said second HSG within the groove 36 after removing said first HSG and said first polysilicon film from the upper surface of the interlayer film (as suggested by JP-H11-284139); and forming an upper electrode comprising forming an upper electrode 39 on said capacitor dielectric film 38.

In re claims 4, 12, 13 and 19, Sung does not teach forming a BPSG over the first interlayer film 29 as the second interlayer film 34.

AAPA, however, teaches utilizing the BPSG as the second interlayer film 120 over the first interlayer film 116 (SiO₂; Figs. 3C-3D) in the DRAM portion.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to replace the silicon oxide of Sung with the BPSG of AAPA used as

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the second interlayer, since by doing so it would provide a better planarization for the subsequent processing steps.

In re claim 9, Sung does not expressly teach the capacitor dielectric film 38 comprising Ta₂O₅ but does suggest that the capacitor dielectric film 38 can be an insulator with a high dielectric constant (col. 7, lines 55-57).

AAPA, however, teaches utilizing a high-dielectric-constant material such as Ta₂O₅ for capacitor dielectric film in DRAM application (page 2, lines 12-13).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the high-dielectric-constant material such as Ta₂O₅, as suggested by AAPA, for capacitor dielectric film in the method of Sung, since by doing so it would improve the performance of the capacitor.

In re claims 14 and 15, the selection of the surface area ratio of the memory cell portion is obvious because it is a matter of determining optimum process condition by routine experimentation for best results for the DRAM performance in conjunction with the consideration the size of CMOS logic circuit portion. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In fact, AAPA teaches that the ration of memory cells 1 to the area of the chip 2 can be 50~60% (Fig. 6A; page 12, lines 14-16). In such situation, the applicants must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05 III

In re claims 20-21, Sung in view of AAPA teaches that the first transistor comprises an n-type transistor having a gate electrode which is made of doped polysilicon and the second transistor comprises a p-type transistor having a gate electrode which is made of doped polysilicon.

Response to Arguments

8. Applicant's arguments filed 11/29/2004 have been fully considered but they are not persuasive.

Applicant's argument is on the ground that "Neither Sung nor JP '139 disclose removing the first polysilicon layer (and removing the *first* HSG layer) from the *upper* surface on the CMOS side, before forming the capacitor dielectric." (second paragraph, page 11)

Contrary to the argument, JP'139 teaches removing the first polysilicon layer 50 (and removing the first HSG layer 52) from the upper surface of the interlayer film 44A before forming the capacitor dielectric 56 (Fig. 7), wherein the interlayer film 44A is formed on the CMOS device comprising a PMOS and a N-MOS (second paragraph, page 9, English version).

Therefore, the teachings of JP '139 would remedy the deficiency in Sung that does not teach forming a capacitor dielectric film 38 on the second HSG film after removing the first HSG and the first polysilicon film from the CMOS logic portion.

For the foregoing reasons, the 103(a) rejection is deemed proper. In addition, Sung also reads on the newly added claim 23.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

Jan 26, 2005

HSIEN-MING LEE
PRIMARY EXAMINER

Lee
1/26/2005